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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,013	03/12/2001	Shigeyuki Maruyama	991489A	7565

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EXAMINER
WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)
09/803,013	MARUYAMA, SHIGEYUKI
Examiner	Art Unit
Alexander O Williams	2826

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2001 and 30 April 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-13, 19 and 20* is/are pending in the application.

4a) Of the above claim(s) *4-13, 19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/472824*.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2,4
4) ☐ Interview Summary (PTO-413) Paper No(s).
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other

Serial Number: 09/803013 Attorney's Docket #: 991489A
Filing Date: 3/12/001:

Applicant: Maruyama

Examiner: Alexander Williams

Applicant's species of figure 5, claims 1-3, in Paper # 6, filed 4/3/02, has been acknowledged.

This application contains claims 4 to 13, 19 and 20 drawn to an invention non-elected without traverse in Paper No. 6.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/472824, filed on 12/28/99.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Frei et al. (U.S. Patent 5,342,999).

1. Frei et al. (figures 1 to 19) specifically figures 10 and 13 show a wafer-level package comprising: a semiconductor wafer **10** having at least one semiconductor chip circuit forming region **60** each including a semiconductor chip circuit and a plurality of chip terminals, said chip terminals including at least one test chip terminal and at least one nontest chip terminal; at least one external connection terminal **(one of 68s)** electrically connected to said at least one non-test chip terminal **(one of 26s)**; at least one redistribution trace **(one of 70s)** provided on said semiconductor wafer, a first end of said redistribution trace being connected to one of said test chip terminals and a second end of said redistribution trace being extended out to a position offset from said one of said chip terminals; at least one testing member **(one of 72s)** provided in an outer region of said semiconductor chip circuit forming region, said second end of said redistribution trace being connected to said least one testing member; and an insulating material **58** covering at least said redistribution trace, said at least one external connection terminal and said at least one testing member being exposed from said insulating material.

2. The wafer-level package as claimed in claim 1, Frei et al. further comprising a sealing resin provided on said insulating material such that top parts of said an external connection terminals and said at least one testing member are exposed from said sealing resin.

3. The wafer-level package as claimed in claim 1, Frei et al.'s at least one external connection terminal and said at least one non-test terminal are electrically connected by an internal redistribution trace in such a manner that said at least one external connection terminal is provided at a position within said semiconductor chip circuit forming region and offset from said at least one non-test chip terminal.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wojnarowski et al. (U.S. Patent # 5,366,906).

1. Wojnarowski et al. (figures 1 to 21) specifically figures 2 and 17 show a wafer-level package **10** comprising: a semiconductor wafer having at least one semiconductor chip circuit forming region **12** each including a semiconductor chip circuit and a plurality of chip terminals **31,38,40**. said chip terminals including at least one test chip terminal and at least one nontest chip terminal **(pads connected within 12, 40)**: at least one external connection terminal **41** electrically connected to said at least one non-test chip terminal: at least one redistribution trace **(lines)** provided on said semiconductor wafer. a first end of said redistribution trace being connected to one of said test chip terminals and a second end of said redistribution trace being extended out to a position offset from said one of said chip terminals: at least one testing member provided in an outer region of said semiconductor chip circuit forming region. said second end of said redistribution trace being connected to said least one testing member: and an insulating material (inherit) covering at least said redistribution trace. said at least one external connection terminal and said at least one testing member being exposed from said insulating material.

2. The wafer-level package as claimed in claim 1. Wojnarowski et al. further comprising a sealing resin (inherit) provided on said insulating material such that top parts of said an external connection terminals and said at least one testing member are exposed from said sealing resin.

3. The wafer-level package as claimed in claim 1. Wojnarowski et al.'s at least one external connection terminal and said at least one non-test terminal are electrically connected by an internal redistribution trace in such a manner that said at least one external connection terminal is provided at a position within said semiconductor chip circuit forming region and offset from said at least one non-test chip terminal.

The listed references are cited as of interest to this application. but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/48.620.784.786.698.211.208.207.203 324/765.537.158R.73.1	6/15/03
Other Documentation: foreign patents and literature in 257/48.620.784.786.698.211.208.207.203 324/765.537.158R.73.1	6/15/03
Electronic data base(s): U.S. Patents EAST	6/15/03

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

6/16/03

Primary Patent Examiner
Alexander O. Williams